## REMARKS

Applicants thank the Examiner for the thorough consideration given the present application. Claims 1-4 and 6-15 are currently being prosecuted. The Examiner is respectfully requested to reconsider his rejections in view of the amendments and remarks as set forth below.

### *Rejections under 35 USC 103*

Claims 1-4 and 6-15 stand rejected under 35 USC 103 as being unpatentable over McGuinness, U.S. Patent 6,104,416, in view of Vinekar, U.S. Patent 5,581,310. This rejection is respectfully traversed.

The Examiner states that McGuinness shows a method of storing an array of digital data into a memory having a plurality of memory pages including dividing the digital data into a plurality of block units with each block unit having a plurality of odd rows and a plurality of even rows, each row having at least one byte. Subsequent odd rows are stored into consecutive storage locations in the first memory section, and subsequent even rows are stored into consecutive storage locations in the second memory section. The Examiner admits that McGuinness does not specifically teach that each memory page has a first memory section and a second memory section. The Examiner relies on Vinekar et al. to describe that each memory page has a first memory section and a second memory section. The Examiner feels that it would have been obvious to modify the device of McGuinness so that each memory page has a first and second memory section as suggested by Vinekar et al.

Applicants disagree that the present claims are obvious over this combination of references. First, with regard to the McGuinness reference, Applicants note that this device is

similar to the prior art device described in Fig. 2 of the present application. As indicated on pages 5 and 6 of the present application, the main drawback of the field-organized storage method is that the reference-top-field-picture and the reference-bottom-field-picture are respectively stored in different field buffers. On the other hand, the reference-frame-picture is composed of a reference-top-field-picture and a reference-bottom-field-picture which are stored in different field buffers. Since the top and bottom fields are stored in different field buffers 2,2', the corresponding top and bottom fields of each macroblock will be stored in different pages. Thus, when a system performs a frame access in order to fetch both the top and bottom field data, it is necessary to cross pages which inevitably cause cross page penalties to occur.

The Examiner admits that McGuinness does not specifically teach that each memory page has a first and second memory section. However, this is a main feature of the present invention. By having two memory sections and storing subsequent odd rows of at least one of the block units into consecutive storage locations of the first memory section and storing subsequent even rows into consecutive storage locations of the second memory section, the present invention can outperform the prior art storage method such as McGuinness' system. That is, by storing the top and bottom fields of each macroblock in the same page, the number of cross pages are substantially reduced and accordingly the cross page penalities are likewise reduced. As a result, the effective DRAM bandwidth can be increased. Accordingly, Applicants submit that the McGuinness device does not show the present invention and, in fact, teaches away from the invention and toward the prior art.

The Examiner relies on Vinekar et al. to show that each memory page has a first memory section and a second memory section. The Examiner feels that it would have been obvious to

modify McGuinness so that each memory page has the two memory sections. The Examiner feels that it would have been obvious because Vinekar teaches the advantage of utilizing every burst mode access, thereby increasing bandwidth and being capable of operating at very high data transfer rates.

Applicants disagree that the teachings of Vinekar et al. can be used to modify the McGuinness device. First, Applicants disagree that Vinekar et al. teaches that each memory page has a first memory section and a second memory section. Although there is shown an odd buffer page and an even buffer page, Vinekar et al. does not describe that the odd buffer page and the even buffer page are in the same memory page. Applicants do not see a description that each memory page has a first memory section and a second memory section. As stated at column 12, lines 47-49, the odd and even field portions of both halves of the image macroblocks are written into different odd and even buffer pages. The paragraph following this further describes the odd buffer page 0, the even buffer page 0, the odd buffer page 1, and the even buffer page 1 as being completely different pages. Vinekar et al. does not describe that each memory page has a first memory section and a second memory section in column 12, line 46 - column 13, line 11, as suggested by the Examiner. Since Vinekar et al. does not teach that each memory page has a first and second memory section, Applicants submit that the Examiner is incorrect in stating that it would be obvious to modify McGuinness in view of Vinekar et al. Accordingly, Applicants submit that claim 1 is not obvious over this combination of references.

Claims 2-4 and 6-9 depend from claim 1 and, as such, are also considered to be allowable. In addition, each of these claims recite certain other features that make them additionally allowable. These include the number of areas in the first and second memory

sections and the number of rows in the block units. Accordingly, these claims are additionally allowable.

Claim 10 is an independent claim that includes the limitations of claim 1 and further describes the digital data as being video data for presenting a picture in a video bit stream. Accordingly, Applicants submit that claim 10 is allowable for the same reasons recited above in regard to claim 1.

Similarly, claim 13 is an independent claim which includes the limitations of claim 1 and further describes the retrieving of the digital data representing the prediction block. Applicants submit that this claim is likewise allowable for the reasons recited above in regard to claim 1. Further, this claim is further allowable in view of the step of retrieving digital data. Accordingly, this claim is likewise allowable.

Claims 11, 12, 14 and 15 depend from allowable claims 10 and 13. In addition, these claims include the limitations found in claims 3 and 8, which depend from claim 1. Accordingly, these claims are likewise considered to be allowable.

*Conclusion*

In view of the above amendments and remarks, it is believed that the claims clearly distinguish over the patent relied upon by the Examiner, either alone or in combination. In view of this, reconsideration of the rejections and allowance of all the claims are respectfully requested.

In the event that any outstanding matters remain in this application, the Examiner is invited to contact the undersigned at (703) 205-8000 in the Washington, D.C. area.

Pursuant to 37 C.F.R. §§ 1.17 and 1.136(a), the Applicants respectfully petition for a one (1) extension of time for filing a response in connection with the present application and the required fee of $120.00 is attached herewith.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Dated: February 28, 2006

Respectfully submitted,

By _____

Joe McKinney Muncy
Registration No.: 32,334
BIRCH, STEWART, KOLASCH & BIRCH, LLP
8110 Gatehouse Road
Suite 100 East
P.O. Box 747
Falls Church, Virginia 22040-0747
(703) 205-8000
Attorney for Applicant

#43,368